

## ABSTRACT

1        This invention describes a unique high-speed implementation  
2 for overflow detection logic to be used in high performance  
3 shifter functions. The overflow logic makes use of parallelism  
4 in combining shift value decoding and mask generation logic with  
5 the logic necessary to propagate data. Designs for both 16-bit  
6 and 32-bit shifters are presented and performance improvement of  
7 the new designs over conventional overflow detection circuits is  
8 demonstrated.